Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Cancel claims 1 - 4.

5. (currently amended) A system, comprising:

a system memory;

a system data bus for providing, in a sequence, read data words retrieved from the system memory and write data words for storage in such system memory, such read data words and write data words being provided on the system data bus at a predetermined system clock rate;

a memory data bus connected to the system memory;

a system memory controller for enabling the system memory to store therein the write data words on the memory data bus at a rate twice the system clock rate and for enabling read data words stored in the system memory to be retrieved therefrom and provided on the memory data bus at twice the system clock rate;

a synchronizer, coupled between the system data bus and the memory data bus, for enabling the read data words retrieved from the system memory at a rate twice the system clock rate to be provided on the system data bus at the system clock rate and for enable write data words provided on the system data bus at the system clock rate to be provided on the memory data bus at twice the system clock rate;

a trace buffer section comprising:

a dual port random access memory having a pair of data ports, such dual port being adapted to store two of the read and write data words provided on the system data bus at the system clock rate and fed concurrently to the pair of data ports into two different memory locations of the dual port random access memory for storage therein at the predetermined system clock rate; and

a trace buffer control system for coupling the read data words provided on the system data bus to one of the pair of ports and for coupling the ~~read~~ write data words provided on the system data bus to the other one of the pair of ports, for controlling the dual port random access memory to enable storage of the read data words and write data words fed to the pair of data ports in the different memory locations, and for enabling such dual port random access memory stored read data words and write data words to be retrieved from memory locations of the dual port random access memory in the same sequence as such read data words and write data words were provided on the system data bus.

6. (currently amended) A system comprising:

a system memory coupled to a memory data bus, such system memory being adapted to store therein write data words provided on the memory data bus, or have read data words stored therein read therefrom provided on the memory data bus, such read data words and such write data words being provided in a sequence on the memory data bus, such system memory being adapted to store the write data words provided on the memory data bus and to provide the read data words on the memory data bus in response to a both a leading edge of a system clock or a trailing edge of the system clock, such system clock having a predetermined clock rate, wherein such read and write data words are provided on the memory data bus at a rate twice the predetermined clock rate;

a trace buffer, comprising:

a dual port random access memory having a pair of data ports, such dual port random access memory being adapted to store two of the read and write data words fed concurrently to the pair of data ports at two different locations in the dual port random access memory in response to the same edge of the system clock, such fed data words being stored in the dual port random access memory at the predetermined clock rate;

a trace buffer control system for coupling read data words from the system memory and provided on the memory data bus to one of the pair of ports of the dual

port random access memory and for coupling ~~read~~ write data words to be stored in the system memory and provided on the memory data bus to the other one of the pair of ports of the dual port random access memory, such read data words and write data words at the pair of ports being stored in the dual port random access memory at sequential locations thereof, such read data words and such write data words being retrievable from the dual port random access memory in the same sequence as such read data words and write data words were provided on the data bus.

7. (currently amended) A system, comprising:

a system memory coupled to a memory data bus, such system memory being adapted to store therein write data words provided on the memory data bus, or have read data words stored therein read therefrom provided on the memory data bus at a rate twice a predetermined system clock rate, such read data words and such write data words being provided on a sequence on the memory data bus;

a trace buffer, comprising:

a dual port random access memory having a pair of data ports, such dual port random access memory being adapted to store two of the read and write data words fed concurrently to the pair of data ports at two different locations in the dual port random access memory for storage therein at the predetermined system clock rate;

a trace buffer control system for coupling read data words from the system memory to one of the pair of ports and for coupling ~~read~~ write data words to be stored in the system memory to the other one of the pair of ports, such read data words and such write data words being retrievable from the dual port random access memory in the same sequence as such read data words and write data words were provided on the data bus.